# New Process for Reclaiming Test Wafers without Copper Contamination

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*A novel wafer reclamation process has been developed to provide copper-contamination-free test wafers. Device manufacturers are concerned with copper contaminated wafers, which result from copper used as a wiring material. A new film removal etchant and polishing slurry have been developed to prevent wafers from being contaminated with copper. These developments have greatly enhanced the reliability of our reclaimed wafers. Furthermore, a method for removing interstitial copper, which penetrated the wafer during the test process, has been developed and successfully applied to the reclamation process.*

## Introduction

In 1996, KOBE PRECISION INC. (KPI), one of overseas group companies of Kobe Steel, started a reclamation business for ϕ150mm and ϕ200mm silicon wafers, using a process collaboratively developed by Kobe Steel's Technical Development Group and KPI[1)-3)]. In 2001, the company started reclamation of ϕ300mm wafers, which are used by state-of-the-art device manufacturers, and the products have currently grown to become our major form factor.

As device feature sizes shrink, conventionally used aluminum wiring has been replaced by copper wiring having higher electrical conductivity[4)]. In the semiconductor industry, however, copper is always of concern as a contaminant, since it easily adheres to the silicon surfaces once it dissolves into hydrofluoric acid solutions, which are frequently used for wet etching and cleaning in device fabrication, and its diffusion rate is very high in silicon crystals.

Devices manufactured onto ϕ300mm wafers, mainly use copper for wiring and it is, therefore, very important to prevent copper contamination in the wafer reclamation process. In addition, copper may also penetrate into silicon wafers, during when the wafers are used as test wafers to monitor device fabrication processes. Therefore, there have been strong demands, from device manufactures to wafer reclaim companies, to remove not only copper on the wafer surfaces, but also copper penetrated inside the wafers.

With this the background, we developed a technology to prevent copper contamination of wafers, both on the surface and inside, and also developed a technology to remove copper penetrated interstitially into the crystal lattices of silicon.

## 1. Wafer reclamation process flow and potential causes for copper contamination

**Figure 1** shows the process flow for ϕ300mm wafer reclamation developed by Kobe Steel and KPI. Wafers are received in a variety of forms. They include wafers with combinations of metallic films, such as Al, W and Ti films, and non-metallic layers, such as silicon oxide layers; wafers with non-metallic layers only; and wafers with patterned films. The wafer reclamation process developed comprises removal of those films, polishing and cleaning. There is a newly developed step for removing copper contamination between the polishing and cleaning steps, of which details are explained in the following.

In our process, removal of films is mainly accomplished by chemical etching and, subsequently, the films remaining after the chemical etching and/or damaged surface layers, such as trace of patterns, are removed by chemical-mechanical polishing. The film removal method is featured by its capability of removing virtually all kinds of films without deteriorating the surface smoothness of mirror finished wafers. After the films are removed,

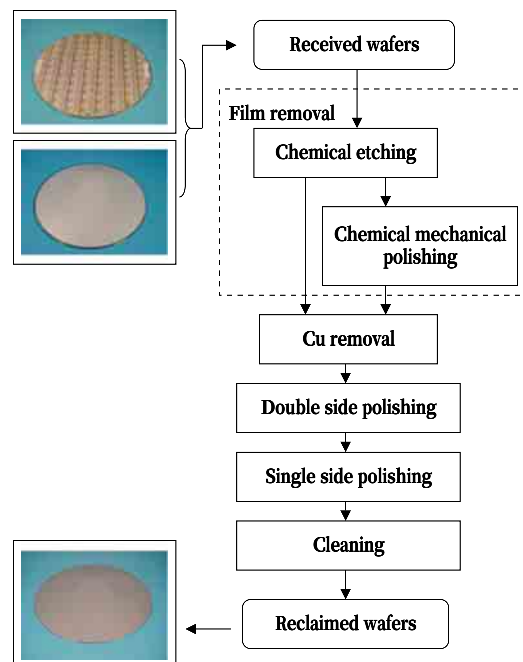


**Fig. 1** Process flow for wafer reclamation

conventional wafer processing methods are basically applied to wafer polishing and cleaning[5].

In the wafer reclamation process shown in Figure 1, the process steps that are most prone to the copper contamination are the chemical etching step, which processes wafers possibly having traces of adhering copper films, and the chemical-mechanical polishing step to remove films remaining on the wafer surfaces. In the chemical etching step, a chemical solution containing hydrofluoric acid is used. Hydrofluoric acid can dissolve almost all the film materials used in device fabrications; however, it has been well known that copper, dissolved into hydrofluoric acid, can precipitate on the wafer surfaces with rather high concentrations[6]. On the other hand, it was pointed out 15 years ago that polishing slurry, having copper concentration in the order of ppm, can cause copper to penetrate into the wafers being polished[7]. Taking the above knowledge into consideration, we developed a technology to prevent copper contamination of wafers, even when copper is dissolved into the solutions and slurry used for the chemical etching and chemical-mechanical polishing. In addition, we developed a method for removing copper, which is diffused interstitially into the crystal lattice of silicon prior to the receipt of the wafers at our site. This article first gives an overview of the preventative measures against copper contamination in the film removal process step. More detailed explanations are provided on the removal of copper diffused interstitially into the crystal lattice of silicon.

## 2. Prevention of copper contamination in the film removal process

Hydrofluoric acid is a convenient etching solution for use in the film removal processes of wafer reclamation processes, since it can dissolve most of the materials used in semiconductor fabrications, but does not dissolve silicon. If silicon wafers are immersed into hydrofluoric solutions containing copper, however, copper adheres to the surfaces of wafer as a result of an electrochemical reaction[6]. In order to suppress the electrochemical reaction, wafer surfaces were protected by combined methods of inactivating copper hydrofluoric solution using chelating agent, suppressing ionic reduction of copper using oxidant and surface protection using surfactant. As a result, even if the etching solution contains as much as 0.2% of copper, copper concentration after etching was managed to be suppressed down to the range between $1\times10^{13}$ and $1\times10^{14}$ atom/cm$^2$. This corresponds to less than 10% of silicon atoms in the top atomic layer of silicon and the process is regarded as capable enough to prevent copper contamination in the etching process.

It has been known for a long time that, if silicon is polished using slurry containing copper, the electrical resistivity of P type silicon increases momentarily and it is clarified[7] that this is caused by copper penetrating into the crystal lattice of silicon during polishing. We developed polishing slurry which removes polysilicon film, silicon nitride film, which tend to remain after the etching process and, at the same time, prevents contamination after polishing, even if copper is contained in the slurry or the films remaining. Copper concentration in polished wafers is suppressed below $5\times10^{11}$atom/cm$^3$, even when the wafers are polished using slurry, containing 2ppm of copper or even when the wafers with and without copper containing films are simultaneously polished, by adequately choosing its abrasive, copper trapping agent and pH adjustment agent[8].

## 3. Behavior of copper in silicon wafers

### 3.1 Behavior of copper in silicon crystal

Weber summarized reports[9] regarding solution and diffusion of copper in crystalline silicon in 1983. The solid solution, diffusion and precipitation of copper in silicon were understood more clearly in the 1990s, when copper started getting attentions as a wiring material of devices. General overviews of the studies were summarized[10, 11] in the early 2000s.

Using the reported data, the diffusion lengths of copper in silicon were calculated for cases in which the silicon is held at temperatures between 273K and 873k for 1 hr (**Figure 2**). In the case of P type wafers, the dopant prevents diffusion of copper and the resulting diffusion length at temperatures below 500K is rather short in wafers with low resistivity, or with high dopant concentrations. At the temperatures above 500K, the diffusion length, for a holding time of one hour, exceeds the thickness of the wafers

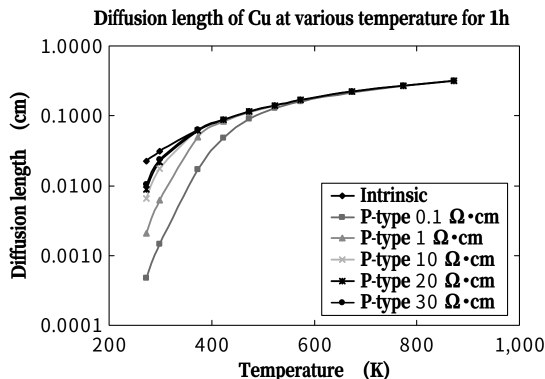


**Fig. 2** Diffusion length of copper in silicon at various temperature for 1 hour

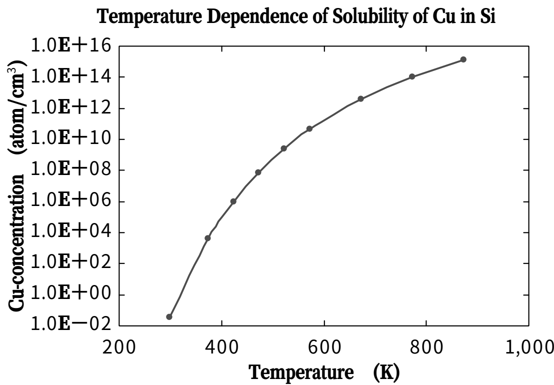


**Fig. 3** Temperature dependence of solubility of copper in silicon

(approximately 0.75mm). Both the results are noteworthy.

Solubility limits of copper in silicon were calculated in a similar manner as described previously and the result is shown in **Figure 3**. The solubility limits at temperatures above 500K, at which the diffusion of copper becomes active, are in the order of $1\times 10^9$ atom/cm$^3$, which correspond to a relative concentrations below $10^{-13}$ comparing to the atomic density of silicon, $5.0\times 10^{22}$ atom/cm$^3$. The concentration is better than the purity of high purity polycrystalline silicon for semiconductor application, called "eleven nines".

Both the calculation results suggest a possibility of precipitating copper inside the wafers at specific points, such as surfaces, by heat treating the wafers at relatively low temperatures around 500K. This further suggests that the copper inside the wafers can be removed, the copper precipitated on the surface is remove by, e.g., cleaning.

In fact, there are methods[12), 13)] proposed to move copper inside the wafers by diffusing copper toward the surfaces and to remove the copper by cleaning and/or etching. Those methods employ mechanical means, such a blasting, to introduce defects to wafer surfaces to enhance copper entrapping effects and, thus, the defects have to be removed to finish the final product wafers. If those methods are applied to φ300mm wafers, which require clean polished surfaces on both the front and back, process steps are inevitably increased and polishing times are extended.

### 3.2 Removal of copper in silicon crystal[14)]

#### 3.2.1 Selection of heat treatment temperatures

There are three conditions for the determination of the heat treatment temperatures, i.e., 1) Diffusion rate of copper, 2) Solid solubility of copper and 3) Oxygen donor formation temperature. Higher temperatures are preferable from the perspective of diffusion rate in order to move copper quickly to the surfaces. However, the higher the temperature the higher the solid solubility of copper becomes, indicating that the concentration of copper remaining inside the wafers becomes higher, even though copper may be moved to the wafer surfaces at a desired speed. In addition, wafers, used widely for device fabrications, contain a certain amount of oxygen, trapped during their crystal pulling processes and the oxygen forms donors in the process of heat treatment. The treatment temperature has to be determined taking those factors into consideration.

**Figure 4** shows changes in resistivities before and after treatments of P type and N type silicon wafers, at temperatures from 373K to 643K, for 20 min and 60 min. In Figure 4, the vertical axis is the change in the rate in % of the difference in specific resistance ⊿R between before and after the heat treatment, divided by the value R before the heat treatment. In the figure, N20 and N 60 denote N type wafers treated for 20 and 60 minute respectively, while P20 and P 60 denote P type wafers treated for 20 and 60 minute respectively. Because oxygen donors are formed at heat treatment temperatures above 573K, increase in resistivity for P type wafers, and decrease in resistivity for N type wafers are observed. Thus, the heat treatment temperature should be kept below 573K, in order to avoid donor formations.

The following experiments were carried out to clarify the effect of temperatures on outer diffusions of copper inside silicon wafers.

It has been known[7)] that, if wafers are polished using slurry containing amine mixed with copper, the copper penetrates into the wafers and increase the specific resistivities of P type wafers. P type wafers, artificially contaminated of their inside, were prepared by exploiting the phenomenon.

The artificially contaminated wafers were held at

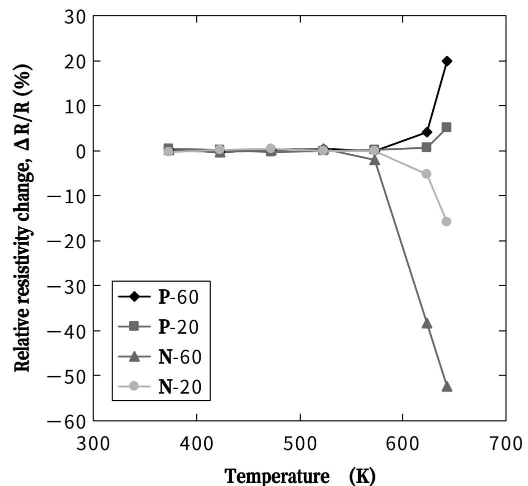


**Fig. 4** Percent resistivity change induced by heat-treatment

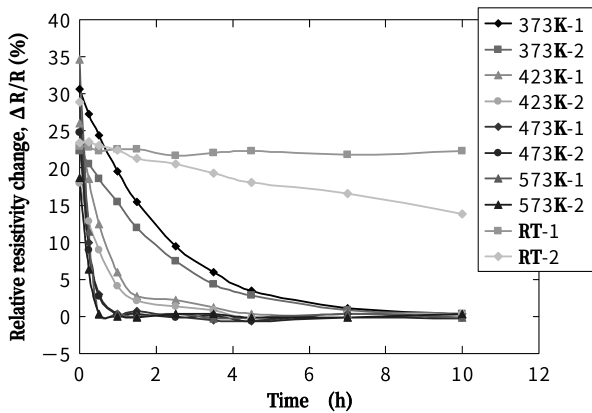


**Fig. 5** Time profile of percent resistivity change returning to initial value

373K, 423K, 473K and 573K to investigate their recoveries of resistivities to the initial values. It was expected that, if the copper penetrated to the inside of wafers is to move to the surface by diffusion, it should dilute the effect of cancelling dopants, and consequently their resistivities should be recovered to their initial states. Two pieces of wafers were evaluated for each condition. The results are shown in **Figure 5**. In Figure 5, the vertical axis is change in the rate in % of the difference in specific resistance ⊿R between before and after the heat treatment divided by the value R before the heat treatment, as in the case of Figure 4. In the data of the figure, the suffix numerals, put after the temperature values, are identifiers of wafers. As expected, recovery time becomes shorter for higher heat treatment temperatures. The result clarifies that copper can be externally diffused in practically short times at temperatures at which oxygen donors are not formed.

In view of the solid solubility of copper at the heat treatment temperatures, the solubility limit at 573K is $1\times10^{11}$ atom/cm$^3$, which corresponds to the purity of semiconductor grade silicon called "eleven nines".

It was concluded, from the above experiments, that the temperature appropriate for outer diffusion is in the range between 423K and 573K, and the corresponding treatment time is in the range from 5 hours to 20 minutes.

### 3.2.2 Study on surface treatment conditions

The recoveries of specific resistivities to initial values shown in Figure 5 are slower that those estimated from the diffusion lengths shown in Figure 2. The thicknesses of wafers used were about 0.72mm and copper right in the middle should be able to reach the surface after diffusing for 0.36mm. The diffusion length at 423K for 1 hr is over 0.8mm, indicating that the majority of copper should be moved to the wafer sub-surfaces. The recovery of specific resistivity, however, takes 4 hours or more. The result suggest that there are other factors, other than diffusion, controlling the movement of copper toward the wafer surfaces. Based on the reports that the native oxide layer affects the outer diffusion of copper in silicon wafers at relatively low temperatures, the effect of surface condition before the heat treatment on the outer diffusion was studied[15].

As in the case of section 3.2.1, P type wafers, artificially contaminated of their inside, were prepared, each of which was respectively treated by water rinse only, and water rinse after immersions in SC1 solution (ammonia and hydrogen peroxide), dilute hydrofluoric solution, SC2 solution (hydrochloric acid and hydrogen peroxide), KOH solution and hydrogen peroxide. Each wafer was held at ambient temperature to investigate the recovery of its specific resistivity. The results are shown in **Figure 6**. In the cases of wafers, treated with water rinse only and hydrofluoric acid, their specific resistivities, which once was increased by copper contamination, recovered only by 20% after 10 days. On the other hand, wafers, immersed in the SC1 solution and KOH solution, recovered their specific resistivities almost to their initial value after one week (168 hours).

Our results are different from the ones reported by Shabani, et. al.[15], in which outer diffusion starts when the native oxide on the wafer surfaces is removed. The causes have not been known yet for the discrepancy of our results from theirs and the differences in outer diffusion rates in wafers processed in different solutions. However, experimental results confirmed that the surface conditions of wafers affect the outer diffusion of copper at relatively low temperatures. Practical value is rather high of the consequence, in which copper inside the wafers can be moved to the surface effectively by diffusion by immersing the wafers in KOH solution and/or SC1 solution prior to the heat treatment.

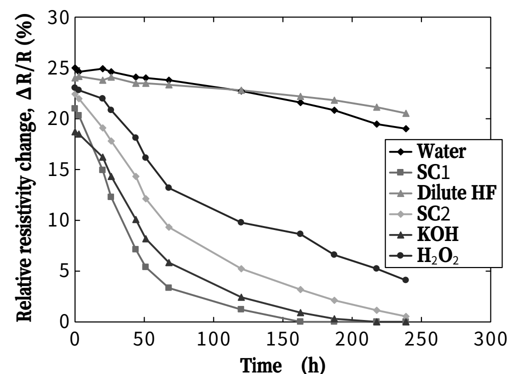


**Fig. 6** Effect of surface treatment on time profile of percent resistivity returning to initial value

### 3.2.3 Removal of copper in the sub-surface

Lastly, the methods for removing copper, diffused to the sub-surface layers, were studied. P type wafers, artificially contaminated on their inside in the same manner as in section 3.1.1, were prepared and each of them was respectively treated by the following four processes. After the treatments, all the wafers are dissolved in a mixture of high purity hydrofluoric acid and nitric acids, to quantitatively measure the amount of copper in the solution by ICPMS and to determine the copper concentrations of the wafers.

Process (1)
1) Heat treatment (523K for 2 hr 30 min)
2) Surface cleaning (hydrofluoric acid and hydrogen peroxide)

Process (2)
1) Surface treatment (immersion into SC1 solution)
2) Heat treatment (523K for 2 hr 30 min)
3) Surface cleaning (hydrofluoric acid and hydrogen peroxide)

Process (3)
1) Heat treatment (523K for 2 hr 30 min)
2) Surface etching (immersion in KOH solution)
3) Surface cleaning (hydrofluoric acid and hydrogen peroxide)

Process (4)
1) Surface treatment (immersion into SC1 solution)
2) Heat treatment (523K for 2 hr 30 min)
3) Surface etching (immersion in KOH solution)
4) Surface cleaning (hydrofluoric acid and hydrogen peroxide)

**Figure 7** shows copper concentrations of wafers processed by the above four treatments. In the figure, the copper concentrations prior to the treatments were estimated from the changes in specific resistivities of each wafer. In addition, in order to verify the validity of the estimations, a piece of wafer, immediately after the artificial contamination, was dissolved into the mixture of hydrofluoric acid and nitric acid and the amount of copper in the solution was determined quantitatively.

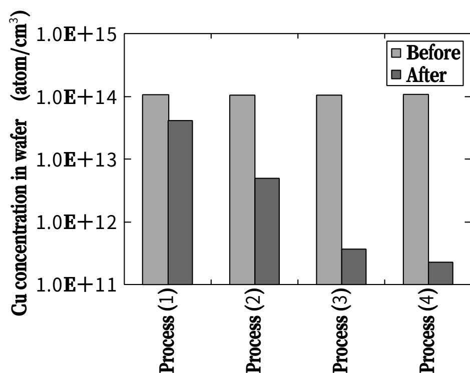


**Fig. 7** Copper concentration in wafer before and after process (1) — (4)

The series of results indicate that copper remains inside the wafers if the wafer surfaces after the heat treatment are merely cleaned and that, in order to remove copper, it is important to etch the sub-surface layer off. Although the heat treatment conditions selected for the experiments can move copper inside wafers to the wafer sub-surfaces, they are not enough to precipitate them on the very surfaces of the wafers.

It is clarified that copper, interstitially penetrated into silicon lattice, can be removed by combinations of a surface modification before heat-treatment, heat treatment, and surface removal after the treatment.

## Conclusions

Device manufacturers are concerned with copper contamination of test wafers and segregate test wafers for use in copper film process from others (non-copper wafers). According to this, device manufacturers are sending wafers with and without copper films to separate reclaim companies. The process, developed by us, provides a high preventative measures, in which wafers with copper films, mixed erroneously with wafers without any copper film, are prevented from contaminating the other wafers. The process is gaining a high reliability from device manufacturers. In addition, application of the present technology has enabled reclamation of wafers with copper films and is expected to grow the wafer reclamation business at KPI.

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